REMARKS/ARGUMENTS

Claims 2-16, 39 and 41 stand allowed, claim 28 is objected to and claims 17-19, 22-27, 29-38 and 40 stand rejected in the outstanding Official Action. Claims 2, 10-19 and 22-41 have been amended and newly written claims 42-56 submitted for consideration. Accordingly, claims 2-19 and 22-56 are the only claims remaining in this application.

The Examiner's indication of allowance of claims 2-16, 39 and 41 is very much appreciated. Applicant has made minor amendments in claims 2 and 10-16, 39 and 41 to correct various minor typographical errors in these claims. The indication of allowance of these claims is very much appreciated. Applicant has also added newly written claims 42-56 which are equivalent to a number of the allowed claims, although the claim language differs slightly. These newly submitted claims are believed to be allowable as well.

Claims 17-19, 22-27, 29-38 and 40 stand rejected under 35 USC §102(e) as being anticipated by Simpson (U.S. Patent 5,469,549). Applicants note that Hugo Simpson and Eric Campbell, the co-inventors of Simpson '549 are also co-inventors of the present application.

The Simpson '549 patent uses a control node mechanism that is suitable for a single processor using cooperative scheduling. As discussed at column 5, lines 22-26, the control node mechanism comprises a set of control nodes which provides control points at which individual activities may wait. Each control node is implemented as a software record which holds an activity number and a Boolean variable named "waiting." When an activity waits on a particular control node, its number is inserted into the activity number field of the control node, and the associated Boolean variable "waiting" is set true. The activity is then de-scheduled and the processor is free to execute other activities. At some later time, the control node may be

"stimmed" by a software process initiated by another activity. The software process reads the control node record. If "waiting" is true, it registers a "current demand for scheduling" on the KEC for the activity number held in the control node, then sets the "waiting" variable faults. If "waiting" is false, no action is taken.

The presently claimed invention uses a control node mechanism which is suitable for multi-processors using co-operative or pre-emptive scheduling. It is implemented using a set of stim-wait channels for each activity. Each stim-wait channel has two Boolean variables, a "stim" bit and a "wait" bit, their values being held in the integrated circuit. Thus, under the presently claimed invention, each stim-wait channel can support an individual control node. When an activity waits on a particular control node, the associated Boolean variable "wait" is set true. When a particular control node is stimmed, the associated Boolean variable "stim" is set true.

This operation is set out in Applicants' amended independent claim 22, which recites that each stim-wait circuit is responsive to a "wait signal" and a "stim signal" to identify when its associated activity is ready to run. Additionally, Applicants' independent claim 22 recites the "next activity logic" to select from the activities that are ready to run "the next activity to be run on the processor."

Thus, each stim-wait supported control node in accordance with the present invention holds **two** Boolean variables in **hardware** (the "stim" and the "wait" circuits), whereas in Simpson, he teaches only that the software record control node holds **one** Boolean variable in **software** (the "wait" signal). Thus, independent claim 22 clearly distinguishes over the Simpson reference, in that it specifies a set of "stim-wait circuits for each activity." This is also true in independent claim 23. Independent claim 24 has a similar distinction from the Simpson

reference, in that it recites "a control node mechanism comprising a set of stim-wait circuits." Applicants note that claims 25-27, 29-38 and 40 all ultimately depend from independent claims 22, 23 or 24 and are similarly patentable over the Simpson reference.

Claims 36 and 37 stand rejected under 35 USC §102 as anticipated by Perotto ("An 8-bit Multitask Micropower RISC Core" August 1994, IEEE Journal of Solid State Circuits). A detailed reading of Perotto indicates that the control variables are used statically (at initialization) to configure the Perotto processor for a specific application. In the present invention, the value of the "stim" and "wait" bits are updated dynamically as activities execute and interact. Perotto also requires that the order of selection is fixed by using a circulating token, whereas in the presently claimed invention, the selection takes into account the changing states of the stim-wait channels as activities execute and interact.

Applicants have amended the language of claims 36 and 37 to more positively recite the above features distinguishing these claims from the Perotto reference. Because Perotto fails to teach Applicants' claimed method steps set out in independent claims 36 and 37, Perotto cannot anticipate or render obvious these claims.

Entry and consideration of newly written claims 42-56 which correspond and are similar to allowed claims 2-16 is respectfully requested.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that remaining claims 2-19 and 22-56 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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